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A Successive Method of Flashing for ADC Networks

Md. Mashrur Islam, Md. Mushfiq ur Rahman and Rubayet Hosen

***Abstract*— In spite of being fastest Flash ADC isn't much popular due to its huge siege and large power consumption. To overcome these problems half flash ADC is introduced in which A/D conversion is done in two steps. Say for an 8-bit system, first the higher 4 bits and then lower 4 bits. So total comparators required is 32. Besides two separate encoder circuit consisting of logic gates and diodes, a 4-bit DAC, a differential amplifier, track and hold circuit etc. is required. So, this system isn't small enough for implementing inside any microcontroller or small digital devices. This paper shows an advanced architecture of A/D converter based on the theory of half flash. The difference is that the convention will happen bit wise. First MSB, then the value of the MSB will be used to generate 2nd MSB. Just a comparator and a differential amplifier is required to generate each bit. No encoder circuit and DAC are required. So, for a n-bit conversion just (2n-1) operational amplifier is required. So, for a 8 bit ADC just 15 op-amp is required. Less amount of op-amp and elimination of encoders and DAC makes the circuit so much smaller and less power consuming and relatively faster which makes it suitable for implementing it inside any microcontroller. This paper explains the contusion, operating principle, errors and process of eliminating errors of a 3-bit ADC.**

***Index Terms*— Flash ADC, Half Flash ADC, DAC, differential amplifier, comparators, propagation delay, Microcontroller.**

I. Introduction

IN Flash Analog to Digital converter the input voltage is compared against some known reference voltages [1]. For a n bit Flash ADC 2^n-1 comparator required [2]. The output of the comparator is fed to an encoder circuit which generates the digital value of the input voltage [1]. The circuit becomes huge for output of higher resolution which causes larger power consumption. So, to reduce the size of the A/D converter half flash technique was introduced [4]. Say for a 4-bit A/D conversion using half flash technique, first a 2 bit conversion takes place having step size $V_{REF}/4$. Then the output is fed to a 2 bit DAC in which four voltage levels can be generated (0 , $V_{REF}/4$, $V_{REF}/2$, $3V_{REF}/4$) which are actually the quantizing levels of the A/D converter. Then a differential amplifier is used to sub struct the input voltage form the output of DAC. The output of the differential amplifier must be within $V_{REF}/4$ and it will be further used for another two-bit conversion having a step size of $(V_{REF}/4)/4$. Hence a 4-bit output is obtained less comparators and smaller encoding circuit [3].

The proposed model of this paper works almost same way. But the differences are that the operation is done bitwise and the application of DAC is removed. First the analog input (V_{IN}) is compared against $V_{REF}/2$. The output of the comparator (MSB) and the analog input voltage is fed to a differential amplifier which is designed such that its output will remain within 0 to $V_{REF}/2$. Then the output of the differential amplifier is compared against $V_{REF}/4$ and like before the output of the comparator and the differential amplifier is fed to another differential amplifier which is designed to keep the output between 0 to $V_{REF}/4$.Process continues till LSB is obtained.

If the circuit was built like half flash, then each stage would require a DAC which will increase the total number of operational amplifiers and hence overall propagation delay would also be increased. As the proposed model has no encoder circuit and DAC so the conversion time would be almost same as typical half flash technique. It's high conversion speed and smaller size makes it more suitable for implementing it in any digital system.

II. Proposed Model

Let's consider Vin is the analog voltage that has to be converted into digital. The reference voltage and IC biasing voltage are both Vcc and Vin ≤ Vcc. As the system discussed here is a three-bit system so the digital value lies between (000) b – (111) b.

First the value of MSB has to be determined. Unlike successive approximation ADC, the input analog voltage is compared against Vcc/2 (i.e. binary 100). In figure 01 if R1=R2 then according to voltage devider law [7] the voltage at the inverting input of the operational amplifier U1 will be V¬cc/2. So if the analog input voltage exceeds Vcc/2 then output of U1 will be equal to Vcc (i.e. bit 2 ; marked by b2 will be set) otherwise it will be zero volt (i.e. b2=0). [Figure 01]

At first stage, the step size was Vcc/2. In order to achieve higher resolution (that is 2nd MSB) step size is reduced into Vcc/4 and if the input voltage is above Vcc/2 then Vcc/2 is subtracted from it is using a differential amplifier constructed by using op-amp U2. The output of the operational amplifier U2 can be measured using superposing theorem.

$$V_2 = - (R_{14}/R_7)(V_{cc}.b_2) + \{R_9(R_{14}+R_7)/R_7(R_8+R_9)\}.V_{in} \quad (1)$$

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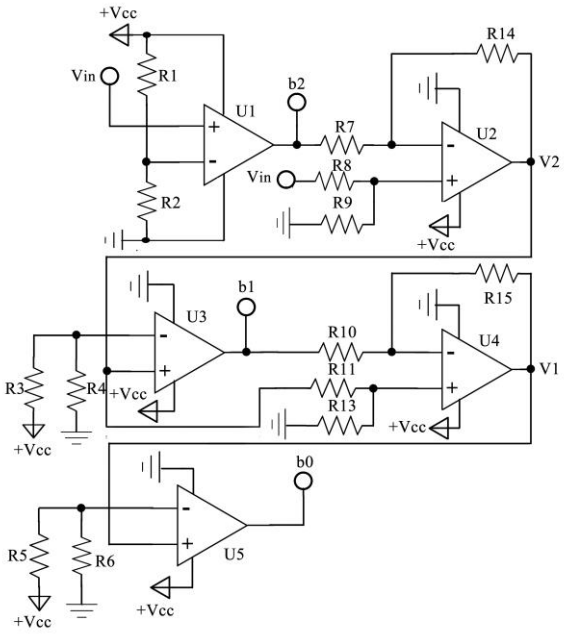

Fig.1. Circuit Diagram of ADC Flash Circuit.

Now if, $R_8=R_{14}$, $R_7=R_9$ and $R_9=2R_8$ then equation 01 becomes,

$$V_2 = -(R_8/R_7)(V_{cc}.b_2) + \{R_7(R_8+R_7)/R_7(R_8+R_7)\}.V_{in}$$
$$\Rightarrow V_2 = -(R_8/2R_8)(V_{cc}.b_2) + \{(R_8+2R_8)/(R_8+2R_8)\}.V_{in}$$
$$\Rightarrow V_2 = V_{in} - (V_{cc}/2).b_2 \quad (2)$$

So, if MSB is set then the initial step size is subtracted from the input. Otherwise the original input voltage is fed to the second comparator. If V_2 exceeds $V_{cc}/4$ then bit 1 (marked by b_1) will be set otherwise it will be zero. [Figure 01]

So like before to obtain higher resolution (i.e. LSB) step size is reduced into $V_{cc}/8$ and if V_2 is greater than $V_{cc}/4$ then $V_{cc}/4$ is subtracted from it using another differential amplifier constructed using an operational amplifier U_4. The output of the differential amplifier U_4 is,

$$V_1 = -(R_{15}/R_{10})(V_{cc}.b_1) + \{R_{13}(R_{15}+R_{10})/R_{10}(R_{11}+R_{13})\}.V_{in} \quad (3)$$

If, $R_{11}=R_{15}$,$R_{10}=R_{13}$ and $R_{13}=4R_{11}$ then equation 03 becomes,

$$V_1 = -(R_{11}/R_{13})(V_{cc}.b_1) + \{R_{13}(R_{11}+R_{13})/R_{13}(R_{11}+R_{13})\}.V_2$$
$$\Rightarrow V_1 = -(R_{11}/4R_{13})(V_{cc}.b_1) + \{(R_{11}+4R_{11})/(R_{11}+4R_{13})\}.V_2$$
$$\Rightarrow V_1 = V_2 - (V_{cc}/4).b_2 \quad (4)$$

Finally, V_1 is compared agains Vcc/8, which gives the value of LSB (i.e. b_0).

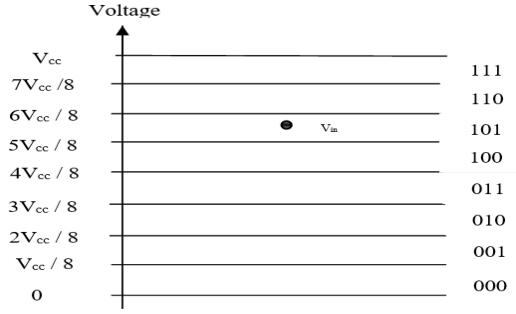

Fig.2. Value Determination of MSB.

The logics are now much simply explained through figure 02. Say, the input voltage is $5.7V_{cc}/8$ which lies between $6V_{cc}/8$ and $5V_{cc}/8$. So, the desired output after ADC conversion should be 101. This means the analog input is in the 6th quantization level. [Figure: 02]

If this input voltage is compared against $V_{cc}/2$ the output of the comparator U_1 will be set. Which means MSB is 1. And the output of the differential amplifier is $.2125V_{cc}$, which lies between $2V_{cc}/8$ and $V_{cc}/8$.

In second step $.2125V_{cc}$ will be compared against $V_{cc}/4$ and the output of comparator U_3 will be zero (i.e. 2nd MSB is zero) and the output of second differential amplifier according to equation 04 is $.2125V_{cc}$ which lies between $2V_{cc}/8$ and $V_{cc}/8$. [Figure: 03]

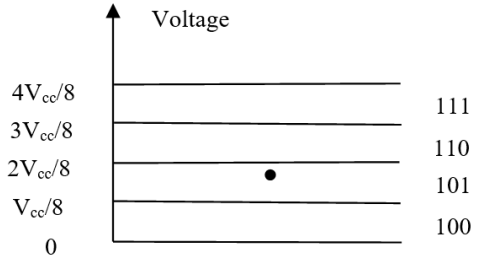

Fig.3. Determining the value of 2nd MSB.

Now finally $.2125V_{cc}$ is compared against $V_{cc}/8$ and the output of comparator U_5 is 1. Which mwans LSB is 1 [Figure: 04]. So, the final output is 101.

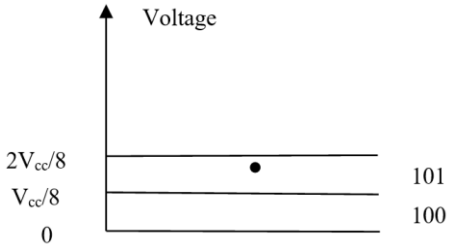

Figure 04: Determining the value of LSB

III. Comparison Among Existing Models

The most important thing for an ADC converter of a specific resolution is the conversion time. This system is faster than successive approximation and digital ramp ADC. Say for example, AVR microcontrollers uses 10bit successive approximation ADC. The conversion takes 13 clock cycles [8, 9]. A 10-bit digital ramp ADC would take maximum 1024 clock cycles. But this proposed model does not take any clock cycle. Only delay is the propagation delay.

But if we compare it with a general flash ADC converter, then it will have comparatively longer propagation delay. Say for an 8-bit conversion this model's propagation delay would consist of 15 op-amp's propagation delay. Whereas, in flash, all comparators are connected parallel and so it causes a very small propagation including an encoder's propagation delay.

In half flash ADC conversion time depends on two comparator stages, two encoders, one DAC, one differential amplifier and one track and hold circuit. So, the conversion time will be significantly large. Say, ADC0820 – 8bit half flash ADC IC provides 2.5µs – 1.5µs conversion time [4]. Now if the proposed model is designed with high speed operational amplifier then the conversion time would be nearly same.

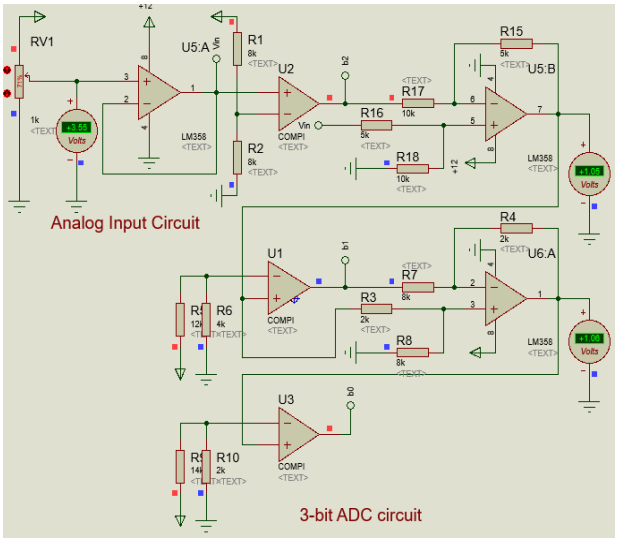

Fig.5.Simulation of proposed ADC circuit using Proteus 8.1.

Now, the second important fact is size. An 8-bit successive approximation ADC would require at least 16 flip flop and some logic gates, a 8 bit DAC, comparator and oscillator. Digital Ramp would require 8-bit counter, 8-bit DAC and comparator. Typical flash would require 255 comparators and a huge encoder circuit. Half flash requires almost 32 comparators [4], encoder circuit, track and hold circuit, DAC, Differential amplifier. But this proposed model would need just 15 op-amps. So, it is surely smallest of all.

IV. Simulation Outputs and Op-Amp Selection

The proposed model is designed into proteous 8.1 using a general comparator model which gives output 5/0 volts and LM358 operational amplifier to make differential amplifier. As it's seen in figure 05, the input analog voltage is 3.55. IC biasing voltage is +12 volts and reference voltage for ADC is 5 volts. Here MSB is set and the output of the differential amplifier connected to MSB (U5:B) is 1.05 which is exactly fulfils equation 02. Then the second MSB is cleared and the output of the differential amplifier connected to MSB (U5:B) is 1.06 which also fulfils equation 04 with a very small error voltage (.01 volts). And finally, 1.06 volt is compared against .625 volt and so the LSB is set which gives the conversion results 101. More conversion results with output voltage in each stage are given in the Table I.

Table-I: A/D conversion results from simulation.

Analog Input	**Circuit Response**				
	Digtal Output	***Differential amplifier output due to MSB***		***Differential amplifier output due to 2nd MSB***	
		Desired	***Obtained***	***Desired***	***Obtained***
3.55 V	111				
	110				
3.55 V	101	1.05		1.06	
	100				
2.15	011				
1.40	010	1.40	1.40	.15	.06

Analog Input	**Circuit Response**				
	Digtal Output	***Differential amplifier output due to MSB***		***Differential amplifier output due to 2nd MSB***	
		Desired	***Obtained***	***Desired***	***Obtained***
.80	001	.80	.80	.80	.81
0 V	000	0 V	.03 V	0 V	.04 V

It is seen from the table that when the input voltage of the operational amplifier is small then the output voltage of it contains an amount of error. In simulation it may be ranging from 1-3 mv. But in practical this same circuit causes almost 16 mv offset value if the input is near zero. Which will cause significant error and makes it impossible to obtain higher resolution.

The main problem is that, in simulation a general comparator model is used which is an ideal comparator. In practical if it made using normal op apm then the maximum output will be always less then reference voltage. That is if the biasing voltage is 5 volt the maximum output of comparator will be less than 5 volts. In case of LM358 it will be nearly 4.86. So, a huge amount error will be happening.

So, the solution is to using rail-to-rail operational amplifier as it works almost like a ideal op-amp [11]. The circuit is further built using TLC2272 rail-to-rail operational amplifier which offer input offset current of .5 pA and input offset voltage of 300 µV. So, the IC biasing voltage and the reference voltage could be kept same (i.e. 5 volts). The output of the comparator lies between .01- 4.99 volts. And the differential amplifiers also work as expected. The output of the differential amplifier measured practically is shown in Table II.

Table-II: Differential amplifier output Using tlc2272.

Analog Input	**MSB representing comparator output**	**Desired output**	**Actual output**
4 V	5 V	1.5 V	1.5V
2 V	0 V	2 V	2 V

V. Practical Implementation

The circuit shown in figure 05 is built using TLC2272 rail to rail op-amp. The input analog voltage is supplied from a potentiometer. Reference is 5 volts. The LED shows the digital output via a buffer which is shown in Figure 06.

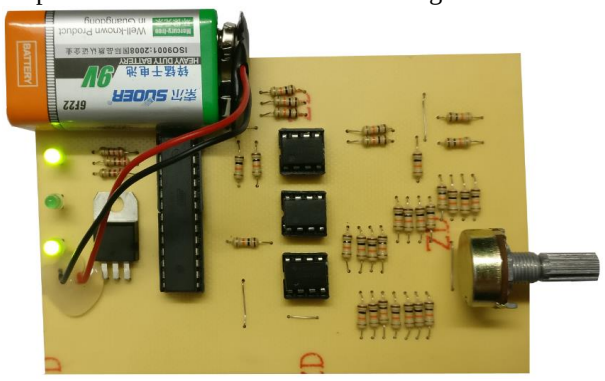

Fig.6. ADC circuit.

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